process on the fly. It is applied to various systems; such as for seismic exploration, communication, and display. It is implemented in various configurations, including integrated circuit and single chip implementations. Filter processing is implemented in various forms; including single bit, incremental, and whole number forms. Signal to noise ratio is enhanced, such as by compositing. Adaptive control is implemented by monitoring the filtered signals.

3.2 Amendments To The Claims

Amend claims 50, 56, 59, 60, 62, 64, 68, 69, 76, 87-92 without acquiescence or prejudice as follows.

--50. (Amended) A [filter processor] receiver system [as set forth in claim 47, further] comprising:

an antenna generating an antenna signal;

an amplifier coupled to the antenna and generating an amplified signal in response to the antenna signal;

a sampling circuit coupled to the amplifier and generating received signal samples in response to the amplified signal;

a single integrated circuit chip signal processor coupled to the amplifier and generating output signal samples in response to the received signal samples, wherein the single integrated circuit chip signal processor is implemented on a single integrated circuit chip, and wherein the single integrated circuit chip signal processor includes

a) an integrated circuit read only memory storing a signal processing program, wherein the integrated circuit read only memory is implemented on the single integrated circuit chip,

b) an integrated circuit input circuit coupled to the integrated circuit read only memory and to the sampling circuit and generating

input signal samples in response to the received signal samples and in response to the signal processing program, wherein the integrated circuit input circuit is implemented on the single integrated circuit chip,

c) an integrated circuit random access memory storing signal processor signal samples, wherein the integrated circuit random access memory is implemented on the single integrated circuit chip,

d) an integrated circuit writing circuit coupled to the integrated circuit read only memory, the integrated circuit input circuit, and the integrated circuit random access memory and writing the signal processor signal samples to the integrated circuit random access memory in response to the input signal samples and in response to the signal processing program, wherein the integrated circuit writing circuit is implemented on the single integrated circuit chip,

e) an integrated circuit accessing circuit coupled to the integrated circuit random access memory and to the integrated circuit read only memory and generating accessed signal samples by accessing the signal processor signal samples from the integrated circuit random access memory in response to the signal processing program, wherein the integrated circuit accessing circuit is implemented on the single integrated circuit chip,

f) an integrated circuit processing circuit coupled to the integrated circuit accessing circuit and to the integrated circuit read

only memory and generating filter processed signal samples by filter processing the accessed signal samples in response to the signal processing program, wherein the integrated circuit processing circuit is implemented on the single integrated circuit chip, and

g) an integrated circuit output circuit coupled to the integrated circuit processing circuit and to the integrated circuit read only memory and generating the output signal samples in response to the filter processed signal samples and in response to the signal processing program, wherein the integrated circuit output circuit is implemented on the single integrated circuit chip; and

a digital to analog converter circuit coupled to the integrated circuit output circuit and generating an analog output signal in response to the output signal samples.

--56. (Amended) A digital signal processor [as set forth in claim 53, further] comprising:

a single integrated circuit chip having a digital signal processor implemented thereon;

an integrated circuit read only memory storing a signal processor program, wherein the integrated circuit read only memory is implemented on the single integrated circuit chip;

an integrated circuit input circuit coupled to the integrated circuit read only memory and generating input signal samples in response to the signal processor program, wherein the integrated circuit input circuit is implemented on the single integrated circuit chip;

an integrated circuit random access memory storing signal processor signal samples, wherein the integrated circuit random access memory is implemented on the single integrated circuit chip;

an integrated circuit writing circuit coupled to the integrated circuit read only memory, the integrated circuit input circuit, and the integrated circuit random access memory and writing the signal processor signal samples to the integrated circuit random access memory in response to the input signal samples and in response to the signal processor program, wherein the integrated circuit writing circuit is implemented on the single integrated circuit chip;

an integrated circuit accessing circuit coupled to the integrated circuit random access memory and to the integrated circuit read only memory and accessing signal processor signal samples stored by the integrated circuit random access memory in response to the signal processor program, wherein the integrated circuit accessing circuit is implemented on the single integrated circuit chip;

an integrated circuit signal processing circuit coupled to the integrated circuit accessing circuit and to the integrated circuit read only memory and generating signal processed signal samples by signal processing the signal processor signal samples accessed by the integrated circuit accessing circuit in response to the signal processor program, wherein the integrated circuit processing circuit is implemented on the single integrated circuit chip;

an integrated circuit output circuit coupled to the integrated circuit signal processing circuit and to the integrated circuit read only memory and generating the digital output signal samples in response to the signal processed signal samples and in response to the signal processor program, wherein the integrated circuit output circuit is implemented on the single integrated circuit chip; and

a digital to analog converter circuit coupled to the integrated circuit output circuit and generating an analog output signal in response to the digital output signal samples.

--59. (Amended) A filter processor ~~implemented~~ on a single integrated circuit chip comprising:

an integrated circuit read only memory storing instructions, wherein the integrated circuit read only memory is implemented on the single integrated circuit chip;

an integrated circuit alterable memory storing operands, wherein the integrated circuit alterable memory is implemented on the single integrated circuit chip;

an integrated circuit input circuit coupled to the integrated circuit read only memory and generating input signals in response to the instructions, wherein the integrated circuit input circuit is implemented on the single integrated circuit chip;

an integrated circuit writing circuit coupled to the integrated circuit read only memory, integrated circuit input circuit, and to the integrated circuit alterable memory and writing operands into the integrated circuit alterable memory in response to the input signals and in response to the instructions, wherein the integrated circuit input circuit is implemented on the single integrated circuit chip;

an integrated circuit processing circuit coupled to the integrated circuit read only memory and to the integrated circuit alterable memory and generating filtered operands in response to the operands and in response to the instructions, wherein the integrated circuit processing circuit is implemented on the single integrated circuit chip, and wherein the integrated circuit processing circuit includes;

a) an integrated circuit multiplier circuit coupled to the integrated circuit read only memory and to the integrated circuit alterable memory and generating product operands by multiplying operands in response to the instructions and

b) an integrated circuit adder circuit coupled to the integrated circuit read only memory and to the integrated circuit multiplier

circuit and generating filtered operands by adding the product operands in response to the instructions; and

an integrated circuit output circuit coupled to the integrated circuit read only memory and to the integrated circuit adder circuit and generating output operands by outputting the filtered operands in response to the instructions, wherein the integrated circuit output circuit is implemented on the single integrated circuit chip.

--60. (Amended) A [wherein the filter processor is a] correlator filter processor implemented on a single integrated circuit chip [as set forth in claim 59] comprising: [; wherein the]

an integrated circuit read only memory [stores the instructions as] storing correlator instructions, wherein the integrated circuit read only memory is implemented on the single integrated circuit chip; [wherein the]

an integrated circuit alterable memory [stores the operands as] storing correlator operands, wherein the integrated circuit alterable memory is implemented on the single integrated circuit chip;

an integrated circuit input circuit coupled to the integrated circuit read only memory and generating input signals in response to the instructions, wherein the integrated circuit input circuit is implemented on the single integrated circuit chip;

an integrated circuit writing circuit coupled to the integrated circuit read only memory, integrated circuit input circuit, and to the integrated circuit alterable memory and writing operands into the integrated circuit alterable memory in response to the input signals and in response to the instructions, wherein the integrated circuit input circuit is implemented on the single integrated circuit chip; [wherein the]

an integrated circuit processing circuit coupled to the integrated circuit read only memory and to the integrated circuit

alterable memory and [generates the filtered operands as] generating correlation filtered operands in response to the correlator operands and in response to the correlator instructions, wherein the integrated circuit processing circuit is implemented on the single integrated circuit chip, and wherein the integrated circuit processing circuit includes

a) an integrated circuit multiplier circuit coupled to the integrated circuit read only memory and to the integrated circuit alterable memory and generating correlation product operands by multiplying correlator operands in response to correlator instructions and

b) an integrated circuit adder circuit coupled to the integrated circuit read only memory and to the integrated circuit multiplier circuit and generating correlation filtered operands by adding the correlation product operands in response to the correlator instructions; and

an [wherein the] integrated circuit output circuit [generates] coupled to the integrated circuit read only memory and to the integrated circuit adder circuit and generating correlator [the] output operands by outputting the [correlation] correlator filtered operands in response to the correlator instructions, wherein the integrated circuit output circuit is implemented on the single integrated circuit chip.

--62. (Amended) A filter processor implemented on a single integrated circuit chip [as set forth in claim 59, wherein the] comprising: [integrated circuit processing circuit is]

an integrated circuit read only memory storing instructions, wherein the integrated circuit read only memory is implemented on the single integrated circuit chip;

an integrated circuit alterable memory storing operands, wherein the integrated circuit alterable memory is

implemented on the single integrated circuit chip;

an integrated circuit input circuit coupled to the integrated circuit read only memory and generating input signals in response to the instructions, wherein the integrated circuit input circuit is implemented on the single integrated circuit chip;

an integrated circuit writing circuit coupled to the integrated circuit read only memory, integrated circuit input circuit, and to the integrated circuit alterable memory and writing operands into the integrated circuit alterable memory in response to the input signals and in response to the instructions, wherein the integrated circuit input circuit is implemented on the single integrated circuit chip;

an integrated circuit iterative processing circuit coupled to the integrated circuit read only memory and to the integrated circuit alterable memory and iteratively generating [the] filtered operands in response to the operands and in response to the instructions, wherein the integrated circuit iterative processing circuit is implemented on the single integrated circuit chip, and wherein the integrated circuit iterative processing circuit includes;

a) an integrated circuit multiplier circuit coupled to the integrated circuit read only memory and to the integrated circuit alterable memory and generating product operands by multiplying operands in response to the instructions and

b) an integrated circuit adder circuit coupled to the integrated circuit read only memory and to the integrated circuit multiplier circuit and generating filtered operands by adding the product operands in response to the instructions; and

an integrated circuit output circuit coupled to the integrated circuit read only memory and to the integrated circuit adder circuit and generating output operands by outputting the

filtered operands in response to the instructions, wherein the integrated circuit output circuit is implemented on the single integrated circuit chip.

--64. (Amended) A filter processor implemented on a single integrated circuit chip [as set forth in claim 59, wherein the integrated circuit alterable memory includes] comprising:

an integrated circuit read only memory storing instructions, wherein the integrated circuit read only memory is implemented on the single integrated circuit chip;

an integrated circuit dynamic random access alterable memory storing operands, wherein the integrated circuit alterable memory is implemented on the single integrated circuit chip; [said filter processor further comprising]

a refresh circuit coupled to the integrated circuit alterable memory and refreshing the integrated circuit alterable memory;

an integrated circuit input circuit coupled to the integrated circuit read only memory and generating input signals in response to the instructions, wherein the integrated circuit input circuit is implemented on the single integrated circuit chip;

an integrated circuit writing circuit coupled to the integrated circuit read only memory, integrated circuit input circuit, and to the integrated circuit alterable memory and writing operands into the integrated circuit alterable memory in response to the input signals and in response to the instructions, wherein the integrated circuit input circuit is implemented on the single integrated circuit chip;

an integrated circuit processing circuit coupled to the integrated circuit read only memory and to the integrated circuit alterable memory and generating filtered operands in response to the operands and in response to the instructions, wherein the integrated circuit processing circuit is implemented on the single integrated circuit chip, and wherein the integrated circuit processing circuit includes;

a) an integrated circuit multiplier circuit coupled to the integrated circuit read only memory and to the integrated circuit alterable memory and generating product operands by multiplying operands in response to the instructions and

b) an integrated circuit adder circuit coupled to the integrated circuit read only memory and to the integrated circuit multiplier circuit and generating filtered operands by adding the product operands in response to the instructions; and

an integrated circuit output circuit coupled to the integrated circuit read only memory and to the integrated circuit adder circuit and generating output operands by outputting the filtered operands in response to the instructions, wherein the integrated circuit output circuit is implemented on the single integrated circuit chip.

--68. (Amended) A filter processor implemented on a single integrated circuit chip [as set forth in claim 65, wherein the integrated circuit processing circuit is] comprising:

an integrated circuit read only memory storing instructions, wherein the integrated circuit read only memory is implemented on the single integrated circuit chip;

an integrated circuit alterable memory storing operands, wherein the integrated circuit alterable memory is implemented on the single integrated circuit chip;

an integrated circuit input circuit coupled to the integrated circuit read only memory and generating input signal samples in response to the instructions, wherein the integrated circuit input circuit is implemented on the single integrated circuit chip;

an integrated circuit writing circuit coupled to the integrated circuit read only memory, integrated circuit input circuit, and to the integrated circuit alterable memory and

writing operands into the integrated circuit alterable memory in response to the input signal samples and in response to the instructions, wherein the integrated circuit input circuit is implemented on the single integrated circuit chip;

an integrated circuit iterative processing circuit coupled to the integrated circuit read only memory and to the integrated circuit alterable memory and iteratively generating [the] filtered operands in response to the operands and in response to the instructions, wherein the integrated circuit processing circuit is implemented on the single integrated circuit chip, and wherein the integrated circuit processing circuit includes;

a) an integrated circuit multiplier circuit coupled to the integrated circuit read only memory and to the integrated circuit alterable memory and generating product operands by multiplying operands in response to the instructions and

b) an integrated circuit adder circuit coupled to the integrated circuit read only memory and generating filtered operands by adding the product operands in response to the instructions; and

an integrated circuit output circuit coupled to the integrated circuit read only memory and generating output operands by outputting the filtered operands in response to the instructions, wherein the integrated circuit output circuit is implemented on the single integrated circuit chip.

--69. (Amended) A filter processor implemented on a single integrated circuit chip [as set forth in claim 65, wherein the integrated circuit processing circuit is] comprising:

an integrated circuit read only memory storing instructions, wherein the integrated circuit read only memory is implemented on the single integrated circuit chip;

an integrated circuit alterable memory storing operands, wherein the integrated circuit alterable memory is implemented on the single integrated circuit chip;

an integrated circuit input circuit coupled to the integrated circuit read only memory and generating input signal samples in response to the instructions, wherein the integrated circuit input circuit is implemented on the single integrated circuit chip;

an integrated circuit writing circuit coupled to the integrated circuit read only memory, integrated circuit input circuit, and to the integrated circuit alterable memory and writing operands into the integrated circuit alterable memory in response to the input signal samples and in response to the instructions, wherein the integrated circuit input circuit is implemented on the single integrated circuit chip;

an integrated circuit multiple loop iterative processing circuit coupled to the integrated circuit read only memory and to the integrated circuit alterable memory and iteratively generating [the] filtered operands with multiple iterative loops in response to the operands and in response to the instructions, wherein the integrated circuit processing circuit is implemented on the single integrated circuit chip, and wherein the integrated circuit processing circuit includes;

a) an integrated circuit multiplier circuit coupled to the integrated circuit read only memory and to the integrated circuit alterable memory and generating product operands by multiplying operands in response to the instructions and

b) an integrated circuit adder circuit coupled to the integrated circuit read only memory and generating filtered operands by adding the product operands in response to the instructions; and

an integrated circuit output circuit coupled to the integrated circuit read only memory and generating output

operands by outputting the filtered operands in response to the instructions, wherein the integrated circuit output circuit is implemented on the single integrated circuit chip.

--76. (Amended) An integrated circuit filter processor [as set forth in claim 71, wherein the integrated circuit alterable memory includes] comprising:

an integrated circuit read only memory storing instructions;

an integrated circuit dynamic random access alterable memory dynamically storing operands; [, said filter processor further comprising]

a refresh circuit coupled to the integrated circuit dynamic random access alterable memory and refreshing the integrated circuit dynamic random access alterable memory;

an integrated circuit input circuit coupled to the integrated circuit read only memory and generating input signals in response to the instructions;

an integrated circuit writing circuit coupled to the integrated circuit read only memory, integrated circuit input circuit, and to the integrated circuit alterable memory and writing operands into the integrated circuit alterable memory in response to the input signals and in response to the instructions;

an integrated circuit processing circuit coupled to the integrated circuit read only memory and to the integrated circuit alterable memory and generating filtered operands in response to the operands and in response to the instructions, wherein the integrated circuit processing circuit includes;

a) an integrated circuit multiplier circuit coupled to the integrated circuit read only memory and to the integrated circuit alterable memory and generating product operands by multiplying operands in response to the instructions and

b) an integrated circuit adder circuit coupled to the integrated circuit read only memory and generating filtered operands by adding the product operands in response to the instructions; and

an integrated circuit output circuit coupled to the integrated circuit read only memory and generating output operands by outputting the filtered operands in response to the instructions.

--87. (Amended) An integrated circuit filter processor system comprising:

an analog to digital converter generating digital communication signals in response to analog communications input signals;

an integrated circuit read only memory storing instructions;

an integrated circuit alterable memory storing operands;

an integrated circuit input circuit coupled to the integrated circuit read only memory and generating input communications signals in response to the instructions;

an integrated circuit writing circuit coupled to the integrated circuit read only memory, integrated circuit input circuit, and to the integrated circuit alterable memory and writing operands into the integrated circuit alterable memory in response to the input communications signals and in response to the instructions;

an integrated circuit processing circuit coupled to the integrated circuit read only memory and to the integrated circuit alterable memory and generating filtered operands in response to the communications operands and in response to the instructions, wherein the integrated circuit processing circuit includes;

a) an integrated circuit multiplier circuit coupled to the integrated circuit read only memory and to the integrated circuit

alterable memory and generating product operands by multiplying communications operands in response to the instructions and

b) an integrated circuit adder circuit coupled to the integrated circuit read only memory and generating filtered operands by adding the product operands in response to the instructions; and

an integrated circuit output circuit coupled to the integrated circuit read only memory and generating output operands by outputting the filtered operands in response to the instructions.

--88. (Amended) An integrated circuit filter processor system as set forth in claim 87:

wherein the filter processor is a correlator filter processor;

wherein the integrated circuit read only memory stores the instructions as correlator instructions;

wherein the integrated circuit alterable memory stores the operands as correlator operands;

wherein the integrated circuit processing circuit generates the filtered operands as correlation filtered operands in response to the correlator operands and in response to the correlator instructions, and

wherein the integrated circuit output circuit generates the output operands by outputting the correlation filtered operands in response to the instructions.

--89. (Amended) An integrated circuit filter processor system as set forth in claim 87, further comprising:

an integrated circuit synchronization circuit generating synchronization signals;

wherein the integrated circuit processing circuit is coupled to the integrated circuit synchronization circuit and

further generates the filtered operands in response to the synchronization signal.

--90. (Amended) An integrated circuit filter processor system as set forth in claim 87, wherein the integrated circuit processing circuit is an integrated circuit iterative processing circuit iteratively generating the filtered operands.

--91. (Amended) An integrated circuit filter processor [as set forth in claim 87, wherein the integrated circuit processing circuit is] system comprising:

an analog to digital converter generating digital communication signals in response to analog communications input signals;

an integrated circuit read only memory storing instructions;

an integrated circuit alterable memory storing operands;

an integrated circuit input circuit coupled to the integrated circuit read only memory and generating input communications signals in response to the instructions;

an integrated circuit writing circuit coupled to the integrated circuit read only memory, integrated circuit input circuit, and to the integrated circuit alterable memory and writing operands into the integrated circuit alterable memory in response to the input communications signals and in response to the instructions;

an integrated circuit multiple loop iterative processing circuit coupled to the integrated circuit read only memory and to the integrated circuit alterable memory and iteratively generating [the] filtered operands with multiple iterative loops in response to the communications operands and in response to the instructions, wherein the integrated circuit processing circuit includes;

a) an integrated circuit multiplier circuit coupled to the integrated circuit read only